# METHOD AND APPARATUS FOR PROCESSING PIXELS BASED ON SEGMENTS

[01] This application claims the priority of Korean Patent Application No. 2003-10044 on 18 February 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

[02] The present invention relates to a memory operating system for encoding and decoding data, and particularly, to a segment-based pixel processing apparatus and a method for effective memory operation.

2. Description of the Related Art

[03] In general, pre-processing or post-processing is performed on an encoded or decoded image signal in order to improve the quality of an image. Here, the pre-processing or post-processing is performed in pixel units.

[04] Referring to FIG. 1, input pixel data is temporarily stored in a frame memory (not shown) in frames units or field units. The pixel data stored in frame or field units is read by a memory for processing. As illustrated in FIG. 1, in general, the pixel data is pre-processed or post-processed through several line memories, starting from the uppermost line of the frame to its lowermost

line from left to right. That is, pixel data within a frame is sequentially pre-processed or post-processed in the sequence of row #0 → row #1 → row #2 → row #3 → row #4, ... , etc.

**[05]** Referring to FIG. 2, let us assume that the neighbor pixels at $n\text{-}1^{th}$ and $n+1^{th}$ rows necessary for pre-processing or post-processing a pixel at an $n^{th}$ row are present right above and under the pixel at the $n^{th}$ row. The pixels at the $n\text{-}1^{th}$, $n^{th}$, and $n+1^{th}$ rows are input to a processor 240 via a first line memory 210, a second line memory 220, and a third line memory 230, respectively.

**[06]** For instance, assuming that an image signal having 720 pixels x 480 lines is present within a frame, a conventional hardware structure for performing low-pass filtering on 3 pixels × 3 pixels requires three line memories capable of storing at least 720 pixels. That is, the conventional hardware structure requires line memory of about 2.2 Kbytes.

**[07]** Accordingly, as more frames are required to be processed and the number of pixels above and under each target pixel increases, a conventional pixel processing method requires more line memory to perform pre-processing or post-processing on the increased number of pixels.

## SUMMARY OF THE INVENTION

**[08]** The present invention provides a segment-based pixel processing method and apparatus in which a frame is divided into several segments and

image processing is performed in segment units, thereby reducing loads on memory.

[09] According to an aspect of the present invention, there is provided a pixel processing apparatus including a frame storage unit in which input pixel data is stored in frame/field units; a line storage unit in which the pixel data, which is stored in the frame storage unit in frame/field units, is stored in line units per vertically-divided segment; a processor that pre-processes or post-processes on the pixel data stored in the line storage unit; and a controller that divides the pixel data within a frame, which is stored in the frame storage unit, into a plurality of segments in the vertical direction, and sequentially stores the pixel data in the line storage unit in the sequence of segments in line units.

[10] According to another aspect of the present invention, there is provided a pixel processing method including dividing pixel data within a frame into a plurality of segments in the vertical direction; sequentially pre-processing or post-processing pixel data in a segment among the plurality of segments in line units, and then, sequentially pre-processing or post-processing pixel data in a next segment in line units; and repeating pre-processing or post-processing on pixel data in the other segments in line units until reaching a segment of a predetermined number.

[11] According to a yet another aspect of the present invention, there is provided a method of processing pixels in a frame that is divided into a plurality of segments, the method including storing pixel data at the first line

of a $k^{th}$ segment in line units; pre-processing or post-processing the pixel data after storing the pixel data in a predetermined number of line units; separately storing the pre-processed or post-processed pixel data, and then, checking whether pre-processing or post-processing is performed on pixel data at the last row of the $k^{th}$ segment or not; checking whether the $k^{th}$ segment is a segment of a predetermined number after the pre-processing/post-processing on the pixel data at the last row; and completing segment-based pixel processing when the $k^{th}$ segment is the segment of the predetermined number, and repeating the pixel processing until reaching the segment of the predetermined number otherwise.

**[12]** In another aspect of the present invention, there is provided a computer-readable recording medium for recording a computer program code for enabling a computer to provide the services of the above methods of processing pixels.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[13]** FIG. 1 illustrates a conventional method of processing pixels within a frame using a pre-processor or a post-processor;

**[14]** FIG. 2 is a block diagram illustrating a structure of an image signal processing apparatus performing the conventional pixel processing method of FIG. 1;

[15] FIG. 3 is a block diagram illustrating a structure of a segment-based pixel processing apparatus according to an exemplary embodiment of the present invention;

[16] FIG. 4 illustrates a method of processing pixels within a frame, according to an exemplary embodiment of the present invention;

[17] FIG. 5 illustrates a method of processing pixels within a frame, according to another embodiment of the present invention; and

[18] FIG. 6 is a flowchart illustrating a method of processing pixels within a frame that is divided into a plurality of segments, according to an exemplary embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[19] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference the accompanying drawings.

[20] FIG. 3 is a block diagram illustrating a structure of a segment-based pixel processing apparatus according to an exemplary embodiment of the present invention.

[21] Referring to FIG. 3, a frame memory 310 temporarily stores input pixel data in frame/field units.

[22] A line memory 320 stores the pixel data, which is stored in the frame memory 310 in frame/field units, in line units per segment in the vertical direction. The size of the line memory 320 is determined by dividing the

length of a frame line by K (K is an integer more than 1). For instance, if a frame having 720 pixels x 480 lines is divided into six segments in the vertical direction, the size of the line memory 320 is 120 pixels × 480 lines. Also, if low-pass filtering is performed in units of 3 pixels × 3 pixels, the number of line memory 320 required is three.

**[23]** A processor 330 performs low-pass filtering, such as pre-processing or post-processing, on the pixel data that is stored in the line memory 320 in line units.

**[24]** An external memory 340 stores the pixel data that is pre-processed or post-processed by the processor 330.

**[25]** A controller 350 reads pixel data, within a frame, which is stored in the frame memory 310, in units of vertically-divided segments, sequentially stores the read pixel data in the line memory 320 in line units per segment, and stores the pixel data, which is pre-processed or post-processed by the processor 330, in the external memory 340.

**[26]** FIG. 4 illustrates a method of processing pixels within a frame, according to an exemplary embodiment of the present invention.

**[27]** Referring to FIG. 4, a frame is divided into several segments, e.g., a first segment, a second segment, ... , etc. Pixel data in the frame is pre-processed or post-processed in the sequence of the first segment → the second segment → ... , etc. Also, the pixel data in each segment is sequentially pre-

processed or post-processed starting from the uppermost line of the frame to the lowermost line as in the conventional pixel processing method shown in FIG. 1. For instance, the pixel data in the first segment is processed in the sequence of pixel data at row #0 → pixel data at row #1 → pixel data at row #2 → pixel data at row #3 → pixel data at row #4, ... , etc. Further, the pixel data at each row is pre-processed or post-processed from left to right.

**[28]** Accordingly, a pixel processing method according to the present invention can be performed with a line memory of remarkably reduced size. If low-pass filtering is performed on an image signal having 720 pixels x 480 lines in units of 3 pixels × 3 pixels, a conventional pixel processing method requires line memory of at least 2.1 Kbytes. However, assuming that the number of pixels at a line within a segment is 120, the size of line memory required in the pixel processing method according to the present invention can be reduced to one sixth, i.e., 360 bytes, of the size of line memory required in the conventional pixel processing method.

**[29]** However, when the frame segments do not overlap one another as shown in FIG. 4, artifacts may occur in pixel data at borders of the segments due to insufficient pixel information during pre-processing/post-processing. To solve this problem, it is possible to divide a frame into several segments as shown in FIG. 5 such that the segments overlap one another by a predetermined number of pixels. FIG. 5 illustrates a method of processing pixels within a frame, according to another embodiment of the present

invention. In this case, although the size of the memory increases slightly, it is possible to prevent artifacts from occurring at the borders of the segments.

**[30]** FIG. 6 is a flowchart illustrating a method of processing pixels within a frame that is divided into a plurality of segments, according to an exemplary embodiment of the present invention.

**[31]** First, let us assume that the pixel data within a frame or field is divided into a plurality of segments in the vertical direction and then, low-pass filtering is performed on the pixel data in units of 3 pixels × 3 pixels. In this case, first through third line memories capable of storing three line data are required. Also, let us assume that the pixel at the uppermost and lowermost lines of the frame will not be processed for convenience.

**[32]** Referring to FIG 6, a total number of rows *n* is initialized to 0 in action 600.

**[33]** In action 610, pixel data at an $n^{th}$ row of a $k^{th}$ segment is input to the frame memory.

**[34]** In action 620, the pixel data at the $n^{th}$ row is input to a first line memory.

**[35]** In action 630, it is checked whether pixel data is stored in all of the three line memories in line units. For instance, it is checked whether n of the $n^{th}$ row is 2. In action 680, if n is not determined to be 2 in action 630, the pixel data stored in the three line memories is shifted to their next memories,

respectively. That is, the pixel data stored in the first line memory is shifted to the second line memory and the pixel data originally stored in the second line memory is shifted to the third line memory.

**[36]** In action 640, if n of the $n^{th}$ row is determined to be 2 in action 630, low-pass filtering, such as pre-processing or post-processing, is performed on the pixel data at the $n\text{-}1^{th}$ row.

**[37]** In action 650, the pre-processed or post-processed pixel data is stored in an external memory.

**[38]** In action 660, it is checked whether pixel data stored at the last row of a $k^{th}$ segment was pre-processed/post-processed. If it is determined in action 660 that pixel data stored at the last row of a $k^{th}$ segment is not pre-processed or post-processed, the pixel processing method returns to action 680 and actions 680 and 610 through 660 are performed again on pixel data at a next row of the $k^{th}$ segment.

**[39]** In action 670, if it is determined in action 660 that pixel data stored at the last row was pre-processed or post-processed, it is checked whether the $k^{th}$ segment corresponds to the last segment *K* of the frame or not (K is an integer more than 1).

**[40]** If it is determined in action 670 that the $k^{th}$ segment corresponds to the last segment *K*, pixel processing in segment units is completed. However, if the $k^{th}$ segment does not correspond to the last segment *K*, the pixel processing method returns to action 610 and pixel processing is performed on pixel data

at a $k+1^{th}$ segment again. In this way, pre-processing or post-processing is sequentially performed in segment units.

**[41]** In conclusion, a frame is divided into segments of a predetermined number and then, pixel data within the frame is sequentially pre-processed or post-processed in the sequence of a first segment, a second segment, ... , etc.

**[42]** While this invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

**[43]** The present invention can be embodied as a computer readable code in a computer readable medium. Here, the computer readable medium may be any recording apparatus capable of storing data that is read by a computer system, e.g., a read-only memory (ROM), a random access memory (RAM), a compact disc (CD-ROM), a magnetic tape, a floppy disk, an optical data storage device, and so on. Also, the computer readable medium may be a carrier wave that transmits data via the Internet, for example. The computer readable recording medium can be distributed among computer systems that are interconnected through a network, and the present invention may be stored and implemented as a computer readable code in the distributed system.

**[44]** As described above, in a pixel processing apparatus and method according to the present invention, a frame is divided into several segments

and pixels within the frame are processed in segment units using a pre-processor or a post-processor, thereby remarkably reducing loads on memory.